REMARKS

Claims 1-21 are pending and at issue. Claims 1-4, 6-8, 11-17 and 19-20 stand rejected as anticipated by Saeed (U.S. Patent No. 6,711,447). The remaining claims each stand rejected under a proposed combination of Saeed and Choi et al. (U.S. Patebt No. 6,233,690). In light of the following remarks, Applicant respectfully asserts that the relied upon art does not teach or suggest the recited subject matter. Reconsideration of the rejection in light of the same is therefore respectfully requested.

Claims 1 and 13 are amended to recite obtaining data on runtime performance of a thread that is indicative of an execution characteristic of the thread and adjusting an operating voltage or an operating frequency of a machine, where the operating voltage and operating frequency is nonzero. This amendment is made to place the clause "of a thread" immediately after the recited "performance" to more clearly indicate the noun which this clause modifies. This amendment further clarifies that the "performance" is indicative of an execution characteristic of the thread. This amendment is supported by the specification at least at page 8, paragraph 0026.

Applicant respectfully traverses the rejection of claims 1-4, 6-8, 11-17 and 19-20 as anticipated by Saeed. Each of the pending claims recite obtaining data on runtime performance of a thread that is indicative of an execution characteristic of a thread, and based on the performance data, adjusting an operating voltage or an operating frequency of the machine, where the operating voltage and operating frequency is nonzero. Saeed fails to disclose obtaining data on runtime performance of a thread that is indicative of an execution characteristic of the thread or adjusting an operating voltage or an operating frequency of a machine where the operating voltage and operating frequency is nonzero, and therefore, cannot anticipate claims 1-4, 6-8, 11-17 and 19-20.

While Saeed discloses a processor power saving feature based on determining the number of threads spawned by a multithreaded application, Saeed fails to disclose obtaining data on runtime performance of a thread, where the data is indicative of an execution characteristic of a thread, much less adjusting a voltage or a frequency based on an execution characteristic of a thread. Instead, Saeed discloses a measure of workload that defines thread performance as the density of multithreaded application threads. This workload does not measure the actual performance of any thread, in any manner.

Generally, Saeed defines workload, or multithreadedness, either as 1) the percentage (%) of threads spawned by a multithreaded application (as opposed to a thread spawned by a single threaded application) over a total number of threads running in a system (see Col. 2 lines 9-13; Col. 2, lines 20-26) or 2) as the number of total threads spawned over the total number of CPU cores (see Col. 2, lines 38-46). In regards to the first definition, Saeed specifically operates under the assumption that threads of multithreaded applications utilize more processing power than threads of single threaded applications (see Col. 57-67). Consequently, Saeed's measure of workload is based on the density of multithreaded application threads, where the workload would be zero if all the threads belong to single threaded applications. However, Saeed never determines the actual runtime performance of any of its threads, in any manner. Saeed avoids analyzing runtime performance, which can vary, and only measures the number of threads and attributes a predetermined, presumed workload. In fact, Saeed fails to even determine if the multithreaded application threads in its system indeed use more processor power than single threaded application threads. In fact, multithreaded application threads may actually under perform single threaded application threads because their execution characteristics (e.g., in the number of instructions executed, the type of instructions executed, or the effect on resources of instructions executed) may be different. For example, when an execution characteristic is defined as a rate of instruction execution, single threaded application threads may execute at a higher rate than multithreaded application threads, and therefore, single threaded application threads may outperform multithreaded application threads during operation. Saeed avoids such an analysis completely.

In regards to the second definition, when the number of threads spawned is less than the number of CPU cores (i.e., when the level of multithreadedness is low), Saeed operates to reduce the number of active CPU cores being used or reduce the amount of power provided to one or more CPU cores. Saeed operates on the notion that the existence of a thread requires one CPU core to service the thread. Consequently, Saeed discloses that when there are less threads in existence than there are CPU cores, then a CPU core is probably not being utilized and should be deactivated or taken to a lower power level. Thus, in these embodiments, similar to those described above, Saeed fails to measure the actual runtime performance of the thread.

Applicants emphasize that the existence of a number of threads, whether the threads are part of single threaded or multithreaded applications, does not provide data on the actual performance of the threads that is indicative of an execution characteristic of the threads. Example execution characteristics may include, but are not limited to, instruction cache misses, data cache misses, instructions executed, branches executed, branch mis-predicts, instruction translation look-up buffer TLB misses, data translation look-up buffer TLB misses, stalls due to data dependency, and data cache write-backs. The method and system of claims 1 and 13, respectively, obtains data on actual runtime performance of a thread that is indicative of an execution characteristic of a thread in order to adjust a voltage or frequency of a machine. Because Saeed fails to disclose obtaining data on runtime performance that is indicative of an execution characteristic of a thread, much less adjusting a voltage or a frequency based on an execution characteristic of a thread, Saeed can not anticipate any of the pending claims.

Applicant respectfully traverses the rejection of claims 5, 9-10, 18 and 21 as obvious in view of Saeed and Choi (U.S. Patent No. 6,233,690). Each of the pending claims recite obtaining from a performance monitor data on runtime performance of a thread that is indicative of an execution characteristic of a thread and based on the performance data, adjusting an operating voltage or an operating frequency of the machine, where the operating voltage and operating frequency is nonzero. Neither Saeed nor Choi discloses data on runtime performance of a thread that is indicative of an execution characteristic of the thread or adjusting an operating voltage or an operating frequency of a machine where the operating voltage and operating frequency is nonzero. Therefore, no combination of Saeed and Choi can render any of the pending claims obvious.

As discussed above, Saeed fails to disclose obtaining performance data indicative of an execution characteristic of a thread, much less adjusting a voltage or frequency based on the execution characteristic. Instead, the Office action relies on Choi to remedy the deficiency. Specifically, the office action relies on Choi for disclosing adjusting a voltage or frequency based on a performance characteristic. The Office action reasons that clock gating implies deactivating a processor such that the processor operates at a zero voltage or a zero frequency and therefore, the process of clock gating an active processor may be read as an adjustment to the voltage or frequency. However, clock gating does not necessarily indicate reducing an operating voltage to zero. Instead, clock gating is only defined as decoupling or

removing the clock signal from a part of a computer system (see Col. 1, lines 23-27), such as a processor. Removing a clock signal from a processor does not mean applying a zero voltage to a processor. For example, when the clock signal is in a high state before the clock signal is removed, the processor may be frozen in a high state, where a high voltage is still applied at a constant level (i.e., without cycling). Moreover, the office action mistakes reducing power consumption for reducing an applied voltage. As specifically disclosed by Choi at Col. 1, lines 27-30, removing a clock signal to a processor reduces power consumption because the processor logic no longer charges and discharges (e.g., based on the clock signal). Thus, while the processor is no longer processing logic based on a clock signal (i.e., charging and discharging), the processor may still be using a voltage (e.g., a constant high voltage).

Furthermore, the office action asserts that frequency is adjusted when the clock signal is gated, implying that absence of a clock signal reads on adjusting an operational frequency. Frequency is the number of repetitions of a periodic process in a unit of time. Gating a clock signal may effectively stop operation of a processor. In this situation, there is no repetition of a process or event, much less repetition of a process or event on a periodic basis. Thus, the transition from the existence of a signal to the non-existence of a signal is not the same as adjusting an existing signal. While the Applicant believes that Choi fails to read on the pending claims, in order to expedite the prosecution of this application, the claims are amended to specifically recite that the operational voltage and frequency are nonzero. Because no combination of Saeed and Choi discloses obtaining data on performance of a thread that is indicative of an execution characteristic of the thread and adjusting an operating voltage or an operating frequency of a machine where the operating voltage and operating frequency is nonzero, no combination of Saeed and Choi can render the pending claims obvious.

CONCLUSION

For the foregoing reasons, Applicant respectfully requests reconsideration and withdrawal of the rejections/objections and allowance of claims 1-21.

While no fees are believed to be due with this response, the Commissioner is authorized to charge any fee deficiency required by this paper, or credit any overpayment, to Deposit Account No. 13-2855.

If there are matters that can be discussed by telephone to further the prosecution of this application, Applicant respectfully requests that the Examiner call its attorney at the number listed below.

Respectfully submitted,

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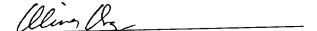
By: 

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